



PSMN4R3-80ES

N-channel 80 V, 4.3 mΩ standard level MOSFET in I2PAK

Rev. 02 — 18 April 2011

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in I2PAK package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switch
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

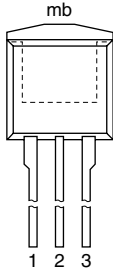
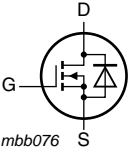
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	80	V	
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	[1]	-	120	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	306	W	
T_j	junction temperature		-55	-	175	°C	
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 13	[2]	-	3.7	4.3	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 100\text{ °C}$; see Figure 12	[2]	-	6.1	7.1	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 75\text{ A}$;	-	28	-	nC	
$Q_{G(tot)}$	total gate charge	$V_{DS} = 40\text{ V}$; see Figure 14 ; see Figure 15	-	111	-	nC	
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 120\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ Ω}$; unclamped	-	-	676	mJ	

[1] Continuous current is limited by package.

[2] Measured 3 mm from package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	drain		

SOT226 (I2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN4R3-80ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

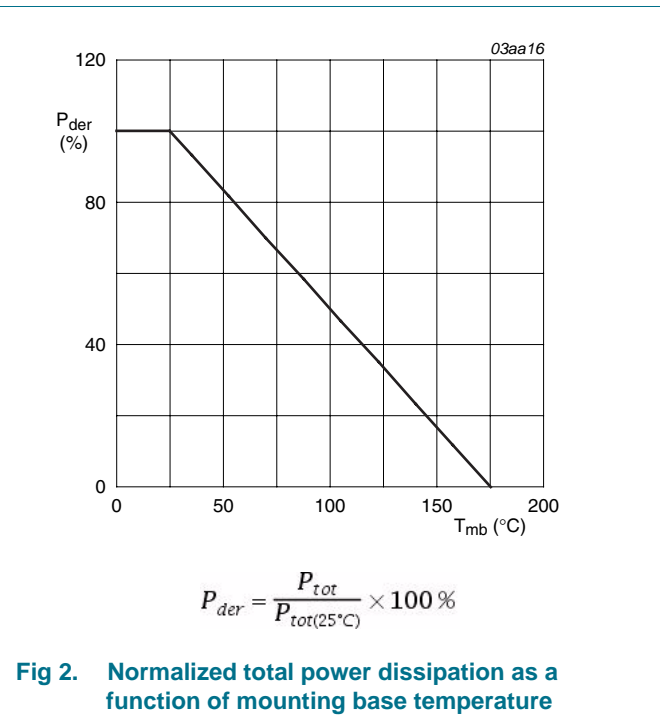
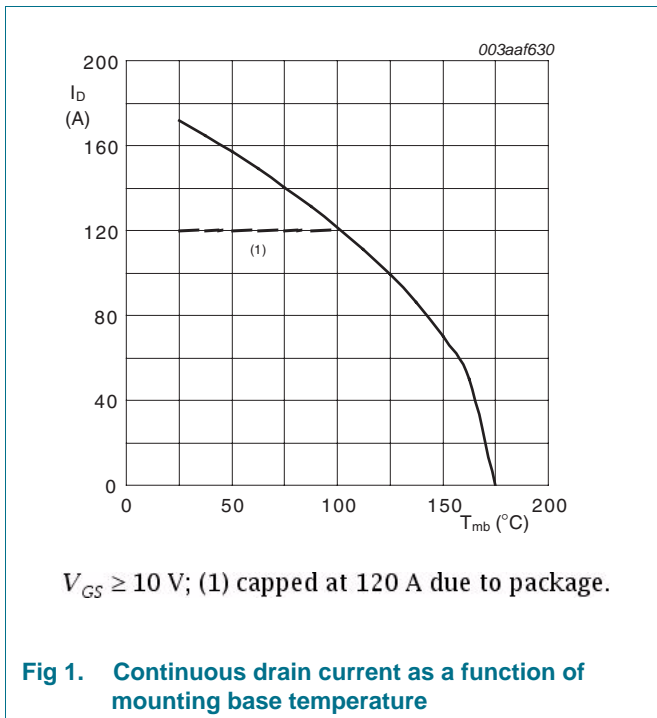
4. Limiting values

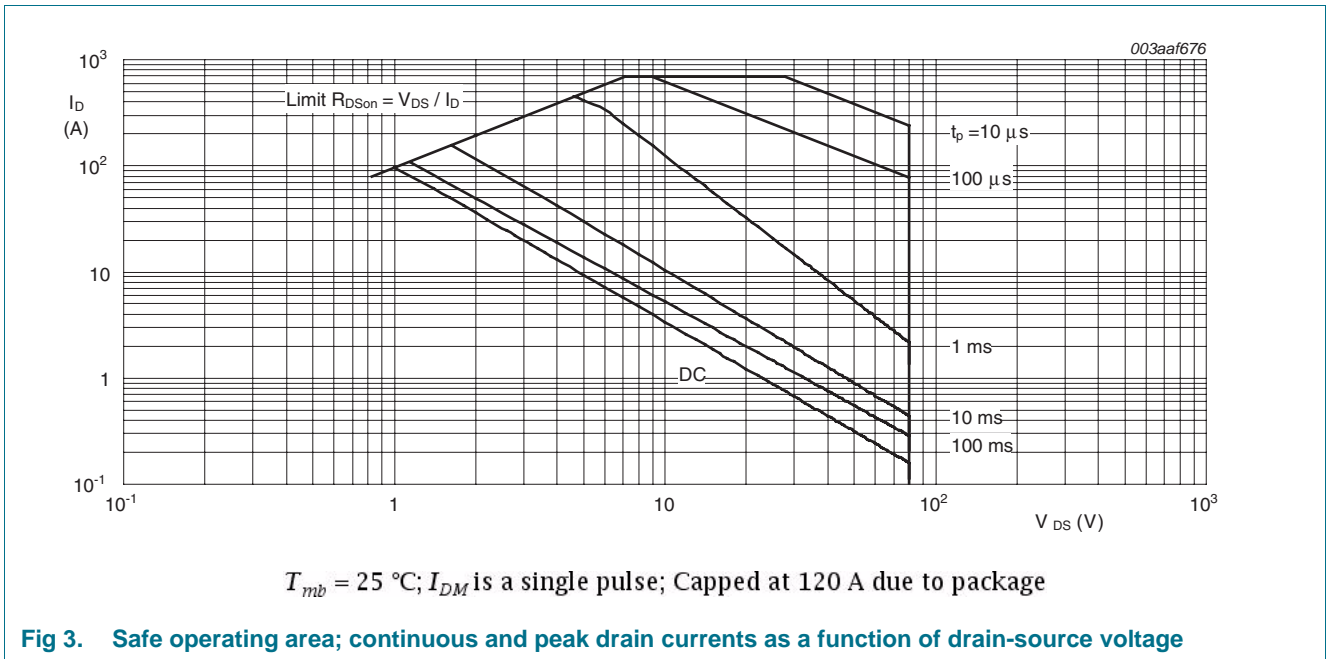
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	80	V	
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	80	V	
V_{GS}	gate-source voltage		-20	20	V	
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$; see Figure 1	[1]	-	120	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$; see Figure 1	[1]	-	120	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	688	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	306	W	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
$T_{sld(M)}$	peak soldering temperature		-	260	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	688	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 120\text{ A}; V_{sup} \leq 80\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped	-	676	mJ	

[1] Continuous current is limited by package.

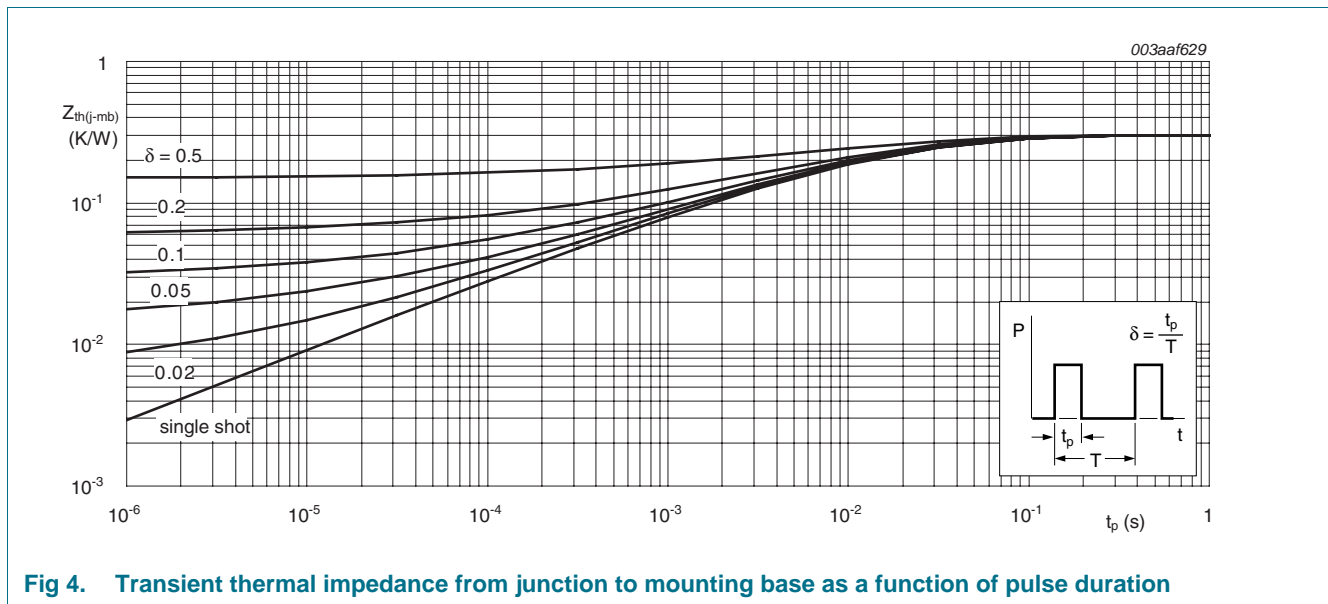




5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.22	0.49	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Vertical in free air	-	60	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	73	-	-	V	
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V	
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 10	1	-	-	V	
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10	-	-	4.6	V	
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	2	3	4	V	
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	10	μA	
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA	
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 12	[1]	-	8.9	10.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	[1]	-	3.7	4.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12	[1]	-	6.1	7.1	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.9	-	Ω	
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	104	-	nC	
		$I_D = 75 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	111	-	nC	
Q_{GS}	gate-source charge		-	38	-	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		-	24	-	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	14	-	nC	
Q_{GD}	gate-drain charge		-	28	-	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V};$ see Figure 14 ; see Figure 15	-	6.1	-	V	
C_{iss}	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16	-	8161	-	pF	
C_{oss}	output capacitance		-	701	-	pF	
C_{rss}	reverse transfer capacitance		-	337	-	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 0.53 \text{ } \Omega;$	-	38	-	ns	
t_r	rise time	$V_{GS} = 10 \text{ V}; R_{G(ext)} = 4.7 \text{ } \Omega;$ $I_D = 75 \text{ A}$	-	29	-	ns	
$t_{d(off)}$	turn-off delay time		-	94	-	ns	
t_f	fall time		-	33	-	ns	

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = 100\text{ A}/\mu\text{s}$;	-	59	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$	-	109	-	nC

[1] Measured 3 mm from package.

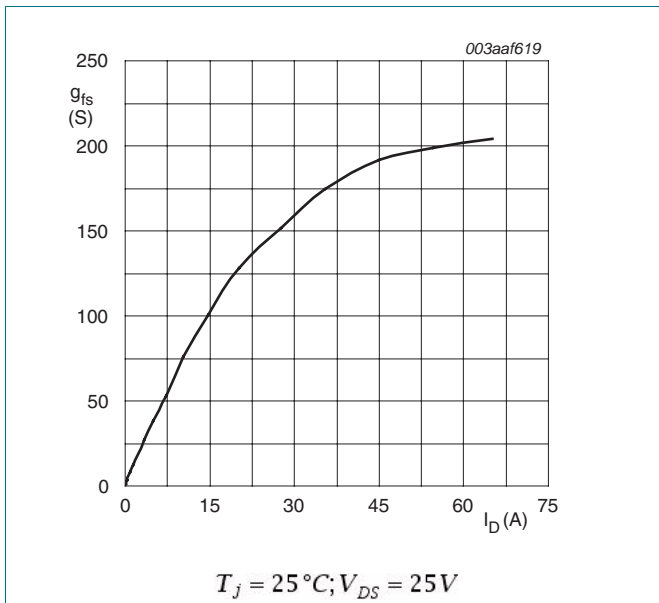


Fig 5. Forward transconductance as a function of drain current; typical values

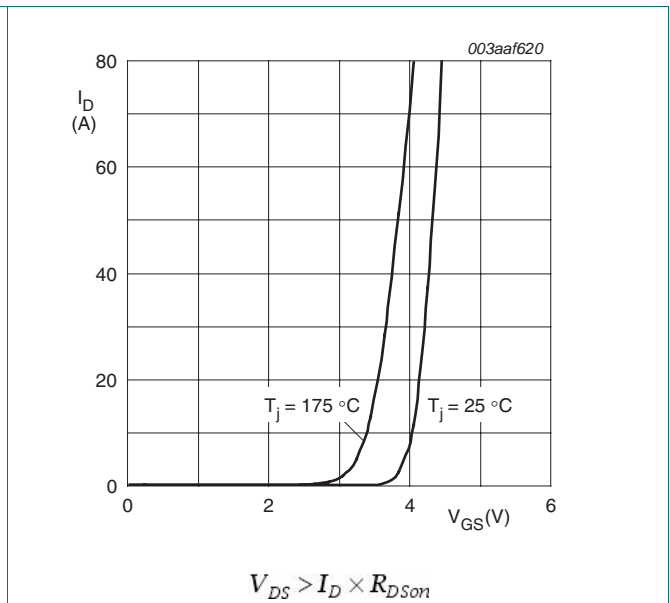


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

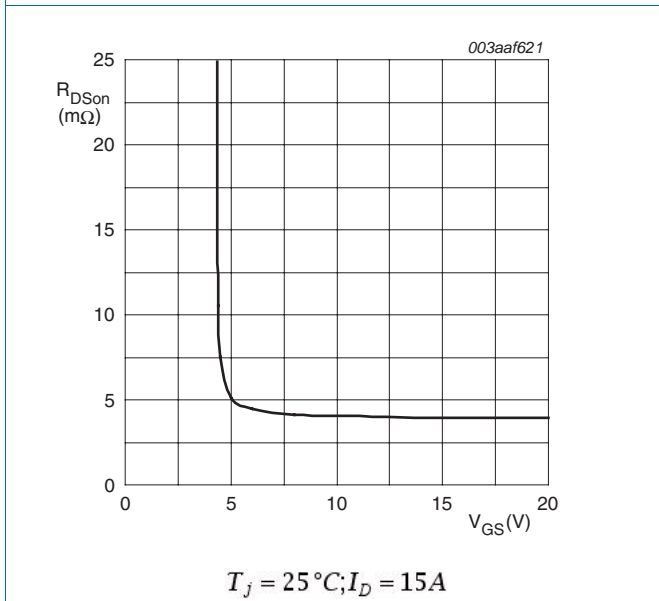


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

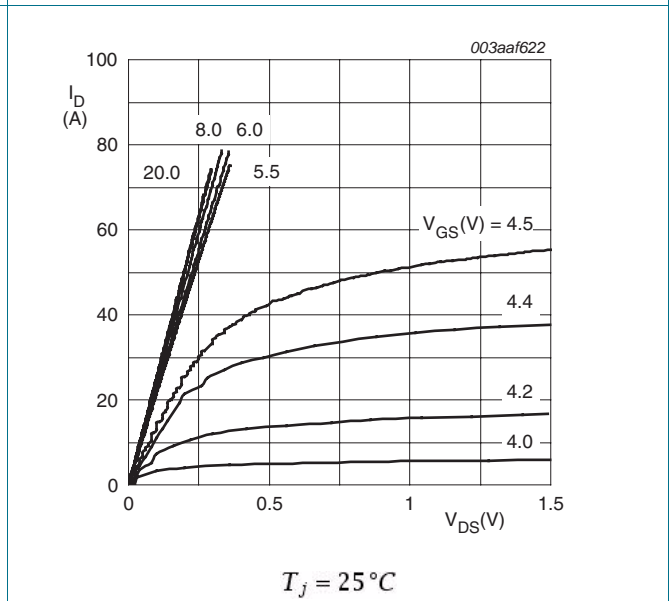
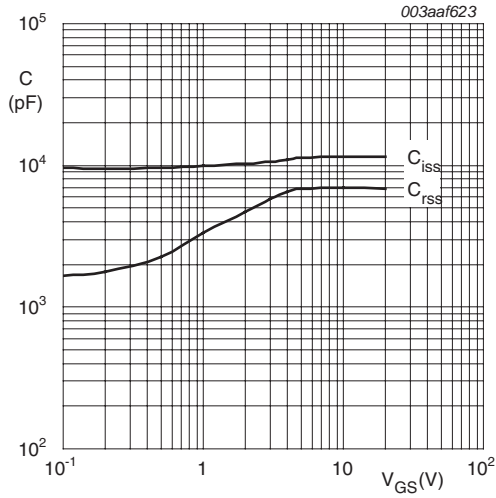
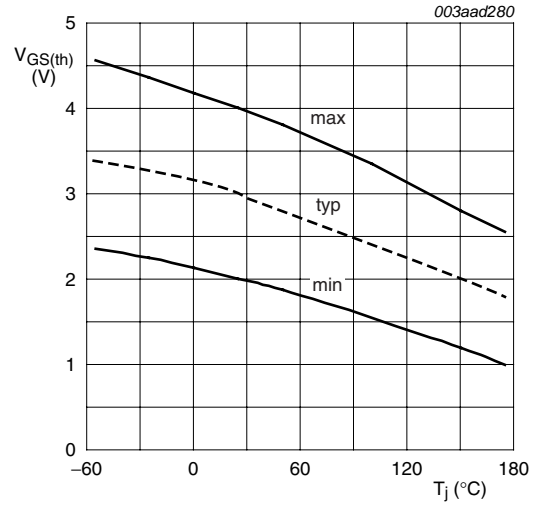


Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



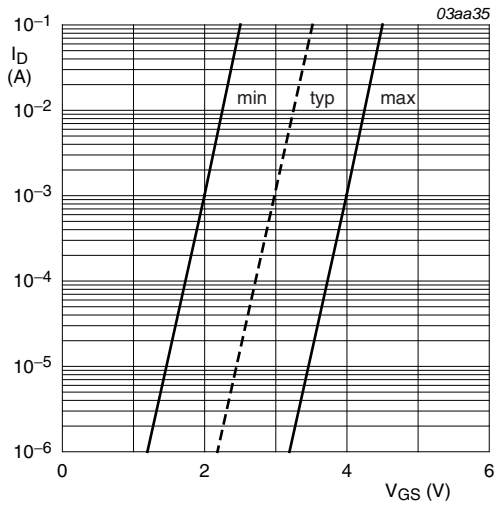
$$V_{DS} = 0V; f = 1MHz$$

Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



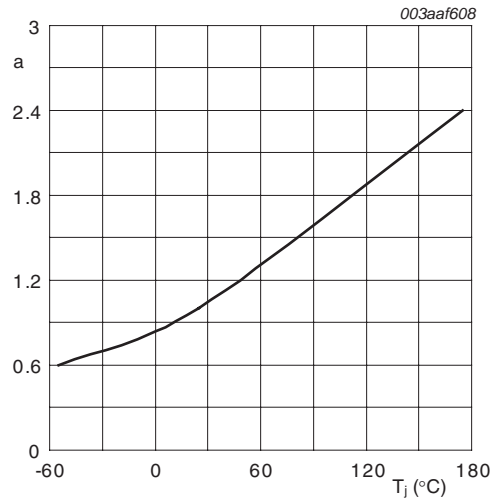
$$I_D = 1 mA; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



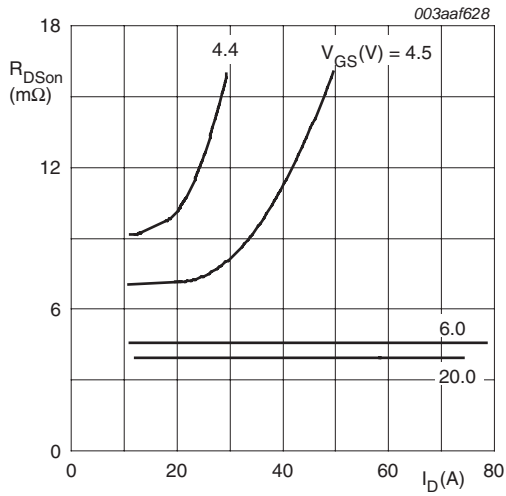
$$T_j = 25^\circ C; V_{DS} = 5V$$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



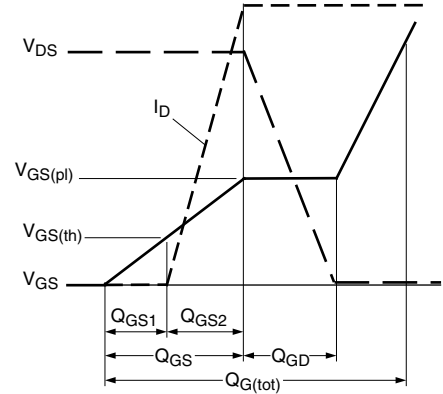
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



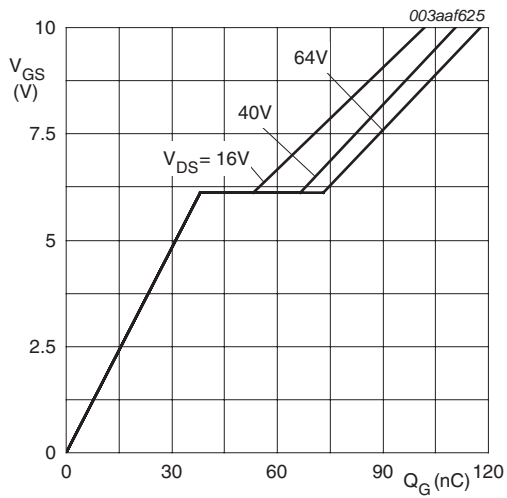
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values



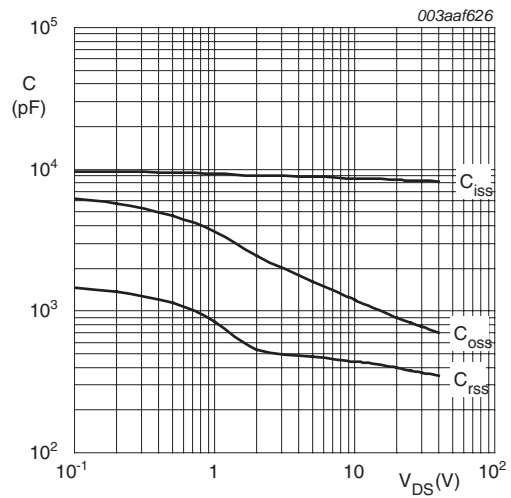
003aaa508

Fig 14. Gate charge waveform definitions



$I_D = 75\text{A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

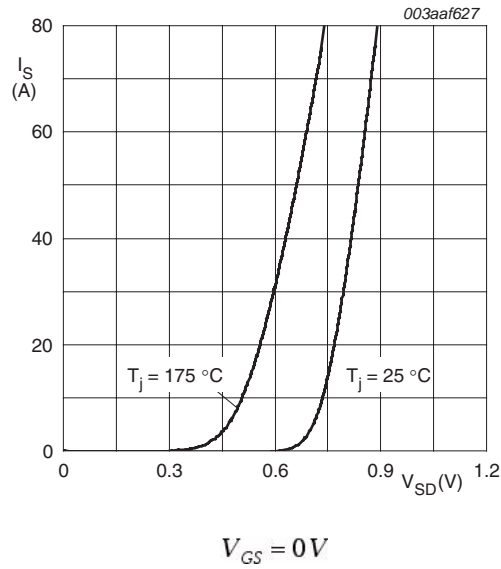


Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

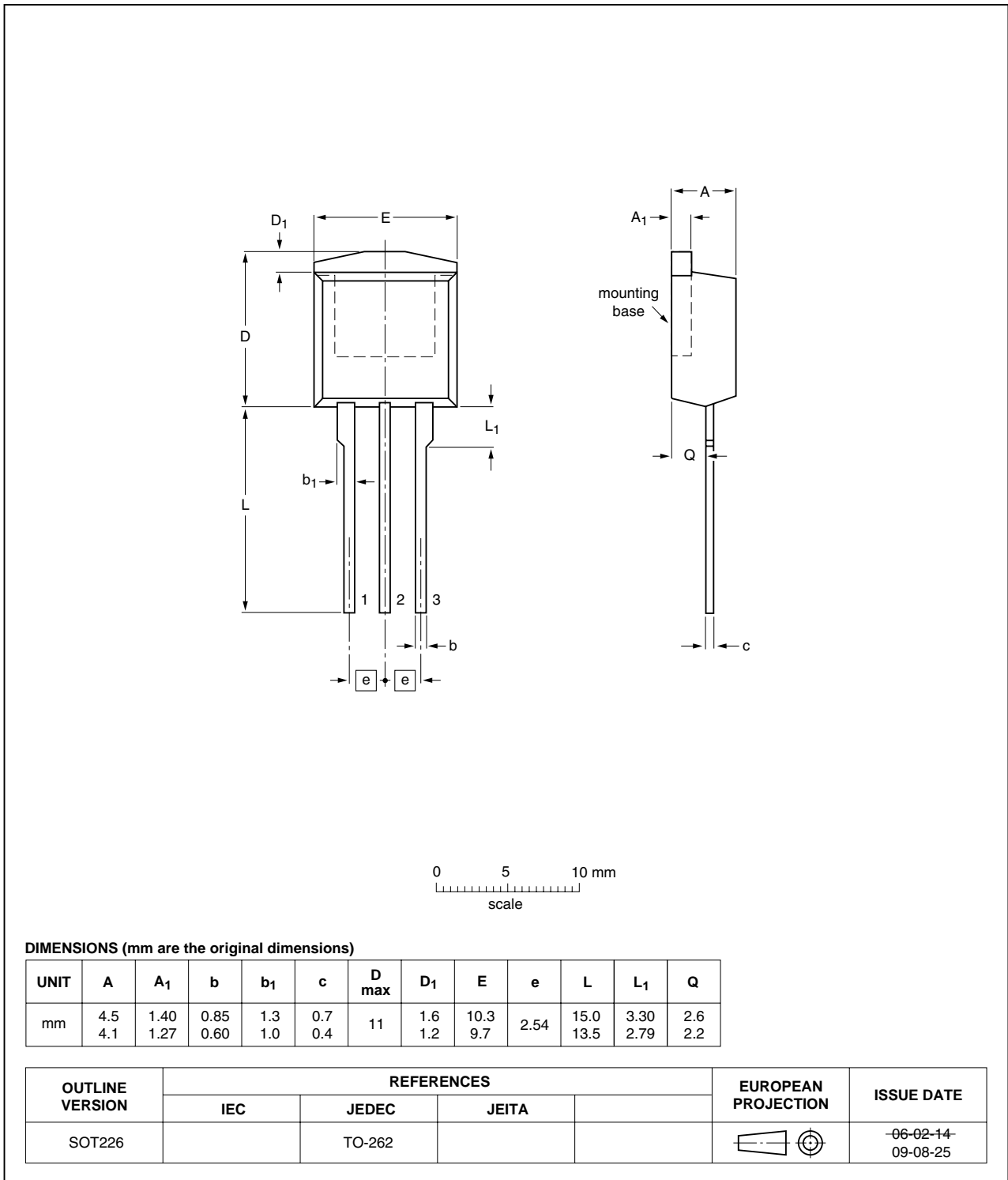


Fig 18. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R3-80ES v.2	20110418	Product data sheet	-	PSMN4R3-80ES v.1
Modifications:	<ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content.			
PSMN4R3-80ES v.1	20101228	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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